REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in substantially the same order in which the corresponding issues were raised in the Office Action.

Status of the Claims

Claims 1-20 are pending. No claims are currently amended. No claims are canceled. No claims are added. No new matter has been added.

Summary of the Office Action

Claims 1-4, 6-12, and 15-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,834,014 to Yoo et al. (hereinafter "Yoo").

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoo in view of U.S. Patent No. 6,538,951 to Janzen et al. (hereinafter "Janzen").

Claims 13 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoo in view of Janzen.

Response to Rejections under 35 U.S.C. § 102(b)

The Office Action rejected claims 1-4, 6-12, and 15-20 under 35 U.S.C. § 102(b) as being anticipated by Yoo. Applicant respectfully requests withdrawal of these rejections because the cited reference fails to disclose all of the limitations of the claims.

CLAIMS 1-7

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Yoo. Applicant respectfully submits that claim 1 is patentable over the cited reference because Yoo does not disclose all of the limitations of the claim. Claim 1, as amended, recites:

> A memory device, comprising:
> an address bus interface;
> an address bus termination circuit that can be enabled or disabled; and
> an address bus termination control signal input, wherein the
> address bus termination control signal input is operable to enable the
> address bus termination circuit when the address bus termination control

signal input is **tied to** a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is **tied to** a second voltage level. (Emphasis added).

Applicants respectfully submit that claim 1 requires that the **address bus termination control signal input be tied to enable/disable the address bus termination circuit**. Yoo fails to disclose this limitation in the claim. Yoo is directed to a memory device for use in a memory system that receives predetermined command/address signals from a memory controller. See Yoo, Abstract. Yoo discloses that an active termination control signal generator *generates a control signal* to control active termination of the at least one data input/output terminal in response to a *chip selection signal* from the memory controller. See col. 2, lines 22-25. The active termination control signal generators of Yoo do not receive control signals from the memory controller chip set 400, but do generate control signals using chip selection signals input into the active termination control signal generators. See col. 6, lines 7-12. The chip selection signal is separately applied from the controller chip set 400. See col. 5, lines 57-63. Accordingly, the inputs of the active termination signal generators *are not tied* to voltage levels, but in fact are connected to a control signal (the chip selection signal) that is either driven high or low based on the chip selection state determined within the controller; thus, requiring a signal to be sent from the controller to the active termination circuit to enable/disable the active termination circuit. Nothing in Yoo disclose the limitation of tying the address bus termination control signal input.

Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 1 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 1 under 35 U.S.C. § 102(b) be withdrawn.

Given that claims 1-4 and 6-7 depend from independent claim 1, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 1-4 and 6-7 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 1-4 and 6-7 under 35 U.S.C. § 102(b) and the rejection of claim 5 under 35 U.S.C. § 103(a) be withdrawn.

CLAIMS 8-16

Claim 8 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Yoo. Applicant respectfully submits that claim 8 is patentable over the cited reference because Yoo does not disclose all of the limitations of the claim. Claim 8, as amended, recites:

> A memory module, comprising:
> a plurality of memory devices coupled to an address bus in **a daisy chain configuration**, each of the plurality of memory devices including
> an address bus interface,
> an address bus termination circuit that can be enabled or disabled, and
> an address bus termination control signal input, wherein the address bus termination control signal input is operable to enable the address bus termination circuit when the address bus termination control signal input is **tied to** a first voltage level, and wherein the address bus termination control signal input is operable to disable the address bus termination circuit when the address bus termination control signal input is **tied to** a second voltage level. (Emphasis added).

Applicant respectfully submits that claim 8 requires a **daisy chain configuration**. Yoo fails to disclose this limitation of the claim. The memory system of Yoo is a stub-bus configuration (See Fig. 2, 4). The stub-bus topology is configured to electrically connect the data signals from the memory control to the data lines of every memory module on the bus, as illustrated in Figures 1, 2, and 4. See col. 1, lines 25-46; col. 2, lines 62-64, col. 4, lines 53-63, col. 5, lines 10-12 and lines 41-43. Nothing in Yoo discloses a daisy chain configuration.

In addition, Applicants respectfully submit that claim 8 also requires **tying the address bus termination control signal input**. Yoo fails to disclose this limitation in the claim. As described above, the inputs of the active termination signal generators *are not tied* to voltage levels, but in fact are connected to a control signal (the chip selection signal) that is either driven high or low based on the chip selection state determined within the controller, which requires that a signal be sent from the controller to the active termination circuit to enable/disable the active termination circuit. Nothing in Yoo disclose the limitation that the **address bus termination control signal input be tied to enable/disable the address bus termination circuit**.

For the reasons stated above, Yoo fails to disclose all of the limitations of claim 8. Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 8 is patentable over the cited reference.

Accordingly, Applicant requests that the rejection of claim 8 under 35 U.S.C. § 102(b) be withdrawn.

Given that claims 9-12 and 15-16 depend from independent claim 8, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 9-12 and 15-16 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 9-12 and 15-16 under 35 U.S.C. § 102(b) and the rejection of claims 13 and 14 under 35 U.S.C. § 103(a) be withdrawn.

CLAIMS 17-20

Claim 17 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Yoo. Applicant respectfully submits that claim 17 is patentable over the cited reference because Yoo does not disclose all of the limitations of the claim. Claim 17, as amended, recites:

> A method, comprising:
> connecting in a **daisy chain configuration** an address bus to a plurality of memory devices on a memory module;
> providing address bus termination circuitry in the plurality of memory devices; and
> enabling the address bus termination circuitry of only one of the plurality of memory devices. (Emphasis added).

Applicant respectfully submits that claim 17 requires a **daisy chain configuration**. Yoo fails to disclose this limitation of the claim. For reasons similar to those described above with respect to claim 8, Yoo does not disclose a daisy chain configuration, but merely a stub-bus configuration.

Given that the cited reference fails to disclose all of the limitations of the claim, Applicant respectfully submits that claim 17 is patentable over the cited reference. Accordingly, Applicant requests that the rejection of claim 17 under 35 U.S.C. § 102(b) be withdrawn.

Given that claims 18-20 depend from independent claim 17, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 18-20 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 18-20 under 35 U.S.C. § 102(b) and the rejection of claims 18-20 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Michael Mallie at (408) 720-8300.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

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